In the Claims

This listing of claims will replace all prior versions, and listings, of claims.

Listing of Claims

1. (currently amended): A method for charge control of a photoflash capacitor comprising the steps of:

detecting a voltage on the photoflash capacitor;

asserting and then latching a recharge signal when the detected voltage is lower than a first reference voltage;

de-asserting and then latching the recharge signal when the detected voltage is higher than a second reference voltage;

asserting and de-asserting a first output signal respectively when the detected voltage is lower and higher than the first reference voltage;

asserting and de-asserting a second output signal respectively when the detected voltage is higher and lower than the second reference voltage;

asserting the recharge signal when the first output signal is asserted, until the second output signal is asserted;

de-asserting the recharge signal when the first output signal is asserted, until the first output signal is asserted;

charging the photoflash capacitor when the recharge signal is asserted; and

providing a pin for connection of a resistive element which determines the first reference voltage.

2. (cancelled)

3. (currently amended): A photoflash capacitor charger operating in conjunction with a microprocessor, comprising:

a transformer receiving a primary input voltage to induce a secondary output voltage on a photoflash capacitor when a recharge signal is asserted;

a recharge controller detecting a voltage on the photoflash capacitor, asserting and then latching the recharge signal when the detected voltage is lower than a first reference voltage, and de-asserting and then latching the recharge signal when the detected voltage is higher than a second reference voltage;

a first comparator circuit asserting and de-asserting a first output signal respectively when the detected voltage is lower and higher than the first reference voltage;

a second comparator circuit asserting and de-asserting a second output signal respectively when the detected voltage is higher and lower than the second reference voltage; and

a latch asserting the recharge signal when the first output signal is asserted, until the second output signal is asserted, and de-asserting the recharge signal when the second output signal is asserted, until the first output signal is asserted;

wherein the first reference voltage is determined by the microprocessor.

4. (cancelled)

5. (currently amended): The photoflash capacitor charger as claimed in claim ~~4~~ 3, wherein the first comparator circuit comprises:

a voltage divider having a first and second resistor connected in series, and receiving the primary input voltage and generating the first reference voltage divided therefrom; and

a comparator having a positive input receiving the first reference voltage and a negative input receiving the detected voltage, and outputting the first output signal;

wherein one of the first and second resistor is adjustable.

6. (currently amended): The photoflash capacitor charger as claimed in claim ~~4~~ 3, wherein the second comparator circuit comprises:

a voltage divider having a first and second resistor connected in series, and receiving the primary input voltage and generating the second reference voltage divided therefrom; and

a comparator having a positive input receiving the detected voltage and a negative input receiving the second reference voltage, and outputting the second output signal.

7. (currently amended): The photoflash capacitor charger as claimed in claim ~~4~~ 3, wherein the latch comprises:

a first and second inverter wherein an input and output of the first inverter are respectively coupled to an output and input of the second inverter;

a third inverter having an input coupled to the output of the second inverter and outputting the recharge signal;

a first switch coupled between the input of the first inverter and the ground, and closed and opened respectively when the first recharge signal is asserted and de-asserted; and

a second switch coupled between the input of the second inverter and the ground, and closed and opened respectively when the second output signal is asserted and de-asserted.

8. (original): The photoflash capacitor charger as claimed in claim 7, wherein each of the first, second and third inverter comprises:

a transistor having a collector as the output and an emitter coupled to the ground;

a current source coupled to the collector of the transistor; and

a resistor having one end as the input and the other end coupled to a base of the transistor.

9. (original): The photoflash capacitor charger as claimed in claim 7, wherein each of the first and second switch is a transistor.

10. (original) The photoflash capacitor charger as claimed in claim 3 further comprising a voltage divider coupled with the photoflash capacitor in parallel, having a first and second resistor connected in series, and generating the detected voltage divided from a voltage difference across the photoflash capacitor.

11. (original): An integrated circuit for recharge control of a photoflash capacitor, comprising:

first, second, third and fourth pins respectively for reception of a ground voltage, primary input voltage, detected voltage from the photoflash capacitor and connection with a resistive element;

a first comparator circuit comprising:

a first comparator having a positive and negative input respectively connected to the fourth and third pin; and

a resistor connected between the second and fourth pin;

a second comparator circuit comprising:

a voltage divider connected between the first and second pins; and

a second comparator having a positive and negative input respectively connected to the third pin and an output of the voltage divider; and

a latch comprising:

a first and second inverter wherein an input and output of the first inverter are respectively connected to an output and input of the second inverter;

a third inverter having an input connected to the output of the second inverter and an output for a recharge signal;

a first switch connected between the input of the first inverter and the first pin; and

a second switch connected between the input of the second inverter and the first pin.

12. (original): The integrated circuit as claimed in claim 11, wherein each of the first, second and third inverters comprises:

a transistor having a collector as the output and an emitter connected to the first pin;

a current source connected to the collector of the transistor; and

a resistor having one end as the input and the other end connected to a base of the transistor.

13. (original): The integrated circuit as claimed in claim 11, wherein each of the first and second switch is a transistor.

14. (original): The integrated circuit as claimed in claim 11 further comprising:

a fifth pin for connection with a primary winding of a transformer; and

a current switch controlled by the recharge signal from the third inverter and connected between the fifth and first pins.